Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A resistance random access memory structure, comprising:
a plurality of word lines in a substrate;
a plurality of reset lines coupled to said word lines;
a dielectric layer on said substrate;
a plurality of memory units in said dielectric layer, each said memory including a bottom electrode, a top electrode, and a resistive thin film between said top electrode and said bottom electrode, said bottom electrodes of said memory units in a same column being coupled to one of said reset lines; and
a plurality of said bit lines on said memory units, said top electrodes of said memory units in a same row being coupled to one of said bit lines.

[c2] 2. The resistance random access memory structure of claim 1, wherein said reset lines are set in said word lines, the ion type of said reset lines being opposite to the ion type of said word lines.

[c3] 3.The resistance random access memory structure of claim 1, wherein said reset lines are set on the surface of said word lines, and wherein the material of said reset

lines is comprised of a metal.

[c4] 4. The resistance random access memory structure of claim 1, further comprising a plurality of word line contact windows in said dielectric layer, wherein each of said word line contact windows are coupled to one of said word lines.

[c5] 5. The resistance random access memory structure of claim 4, further comprising a plurality of doped regions in said word lines, wherein each of said doped regions are coupled to one of said word line contact windows, and wherein an ion types of said doped regions and said word lines is same.

[c6] 6. The resistance random access memory structure of claim 1, further comprising a plurality of reset line contact windows in said dielectric layer, each of said reset line contact windows being coupled to one of said reset lines.

[c7] 7. The resistance random access memory structure of claim 1, wherein said memory units in a same column are set on a surface of said reset lines.

[c8] 8. The resistance random access memory structure of claim 1, wherein said resistive thin film material is resistance-reversible.

[c9] 9. The resistance random access memory structure of claim 1, wherein said resistive thin film material is selected from colossal magneto resistive thin films and oxidation thin films having Perovskite structure.

[c10] 10. A method for fabricating a resistance random access memory, comprising the steps of:
forming a plurality of word lines in a substrate;
forming a plurality of rest lines, each of said rest lines being coupled to one of said word lines;
forming a plurality of memory units on said substrate, each of said memory unit including a bottom electrode, a top electrode, and a resistive thin film between said top electrode and said bottom electrode, said bottom electrodes of said memory units in a same column being coupled to one of said reset lines;
forming a dielectric layer on said substrate, said dielectric layer exposing said memory units; and
forming a plurality of bit lines on said memory units, said top electrodes of said memory units in a same row being coupled to one of said bit lines.

[c11] 11. The method for fabricating a resistance random access memory of claim 10, wherein said reset lines are set in said word lines, and wherein an ion type of said reset lines is opposite to an ion type of said word lines.

[c12] 12. The method for fabricating a resistance random access memory of claim 10, wherein said reset lines are set on the surface of said word lines, and wherein a material of said reset lines is comprised of a metal.

[c13] 13. The method for fabricating a resistance random access memory of claim 10, wherein said steps of forming said memory units and said bit lines include:
forming a stack layer on the surface of each of said reset lines;
forming said dielectric layer on said substrate, said dielectric layer exposing said stack layers;
forming a conducting layer on said dielectric layer and said stack layers; and
patterning perpendicularly to said word lines said conducting layer and said stack layers to form said bit lines and said memory units.

[c14] 14. The method for fabricating a resistance random access memory of claim 10, after said step of forming said dielectric layer, further comprising a step of forming a plurality of word line contact windows in said dielectric layer, wherein each of said word line contact windows is coupled to one of said word lines.

[c15] 15. The method for fabricating a resistance random ac-

cess memory of claim 10, after said step of forming said word lines, further comprising a step of forming a doped region in each of said word line, wherein each of said doped regions is coupled to one of said word line contact windows, and wherein an ion types of said doped regions and said word lines is same.

[c16] 16. The method for fabricating a resistance random access memory of claim 10, after said step of forming said dielectric layer, further comprising a step of forming a plurality of reset line contact windows, wherein each of said rest line contact windows is coupled to one of said reset lines.

[c17] 17.The method for fabricating a resistance random access memory of claim 10, wherein said resistive thin film material is resistance-reversible.

[c18] 18.The method for fabricating a resistance random access memory of claim 17, wherein said resistive thin film material is selected from colossal magneto resistive thin films and oxidation thin films having Perovskite structure.